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APPLICATION FOR LETTERS PATENT

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Memory Circuitry and Method Of Forming Memory Circuitry

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INVENTOR

Belford T. Coursey

ATTORNEY'S DOCKET NO. MI22-1461

EL 465686178

Memory Circuitry and Method Of Forming Memory Circuitry

TECHNICAL FIELD

This invention relates to memory circuitry and to methods of forming memory circuitry.

BACKGROUND OF THE INVENTION

Memory circuitry in semiconductor fabrication is formed to include an array area where individual memory cells are typically fabricated in a dense repeating pattern, and a peripheral area where peripheral circuitry which is operatively configured to write to and read from the memory array is fabricated. Peripheral circuitry and array circuitry are typically largely fabricated at the same time. Further the memory cell capacitors within the memory array are commonly fabricated to be vertically elongated, sometimes in the shape of cups or containers, in order to maximize the available surface area for individual capacitors for storage capacitance. The electronic components or devices of the peripheral circuitry are not typically as vertically elongated, thereby creating topography problems in the fabrication due to portions of the memory array circuitry being fabricated significantly elevationally higher than portions of the peripheral circuitry.

The invention was principally motivated in addressing or overcoming problems associated with this issue, and in the fabrication

of capacitor-over-bit line dynamic random access memory circuitry. However, the invention is in no way so limited, and is applicable without limitation to these problems or objectives, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention comprises memory circuitry and methods of forming memory circuitry. In but one implementation, a method of forming memory circuitry having a memory array having a plurality of memory capacitors and having peripheral memory circuitry operatively configured to write to and read from the memory array, includes forming a dielectric well forming layer over a semiconductor substrate. A portion of the well forming layer is removed effective to form at least one well within the well forming layer. An array of memory cell capacitors is formed within the well. The peripheral memory circuitry is formed laterally outward of the well forming layer memory array well.

In one implementation, a dielectric well forming layer is formed over a semiconductor substrate. A portion of the well forming layer is removed effective to form at least one well within the well forming layer. A capacitor storage node forming layer is formed within the well. An array of capacitor storage node openings is formed within the capacitor storage node forming layer within the well. Capacitor storage

node electrodes are formed within the capacitor storage node forming layer openings. After forming the capacitor storage node electrodes, at least some of the capacitor storage node forming layer is removed from within the well. Peripheral memory circuitry is formed laterally outward of the well.

In one implementation, memory circuitry includes a semiconductor substrate. A plurality of word lines is received over the semiconductor substrate. An insulative layer is received over the word lines and the substrate. The insulative layer has at least one well formed therein. The well has a base received over the word lines. The well peripherally defines an outline of a memory array area. Area peripheral to the well includes memory peripheral circuitry area. A plurality of memory cell storage capacitors is received within the well over the word lines. Peripheral circuitry is received within the peripheral circuitry area and is operatively configured to write to and read from the memory array.

Other implementations are contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with an aspect of the invention.

Fig. 2 is a diagrammatic sectional view of the Fig. 1 semiconductor wafer fragment at the one processing step of Fig. 1 but taken through a different section of the wafer fragment.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 1.

Fig. 4 is a top plan view of the Fig. 3 wafer fragment.

Fig. 5 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that depicted by Fig. 3.

Fig. 6 is a view of the Fig. 5 wafer fragment at a processing step subsequent to that depicted by Fig. 5.

Fig. 7 is a view of the Fig. 6 wafer fragment at a processing step subsequent to that depicted by Fig. 6.

Fig. 8 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that depicted by Fig. 7.

Fig. 9 is a view of the Fig. 8 wafer fragment at a processing step subsequent to that depicted by Fig. 8.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 9.

Fig. 11 is a view of the Fig. 10 wafer fragment at a processing step subsequent to that depicted by Fig. 10.

Fig. 12 is a view of the Fig. 11 wafer fragment at a processing step subsequent to that depicted by Fig. 11.

Fig. 13 is a view of the Fig. 12 wafer fragment at a processing step subsequent to that depicted by Fig. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring initially to Figs. 1 and 2, a semiconductor substrate in the form of a wafer fragment is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Further in the context of this document, the term "layer" encompasses both the singular and the plural.

In only a preferred embodiment, dynamic random access memory circuitry is fabricated and described. Semiconductor wafer fragment 10

comprises a bulk monocrystalline substrate 12 having an array of word lines 14 formed thereover. Such are shown as comprising a gate oxide layer 16, an overlying conductively doped polysilicon layer 18, an overlying silicide layer 20, and an insulative cap 22. Anisotropically etched insulative sidewall spacers 23 are received about word lines 14. Capacitor storage node plugs 24 are received between the illustrated word lines; and constitute exemplary storage node contact locations as will be apparent from the continuing discussion. An array of digit lines 26 (Fig. 2) is formed over word lines 14. An insulative layer 29 is received between digit lines 26 and substrate 12, and exposes a digit line contact location 28 between the middle two illustrated word lines. An example material for layer 29 is undoped SiO_2 deposited by decomposition of tetraethylorthosilicate. An exemplary thickness is from about 300 Angstroms to about 500 Angstroms. Suitable source/drain constructions (not shown) would be provided relative to substrate 12 as is conventional, or as might be developed in later generation technologies.

A dielectric well forming layer 30 is formed over semiconductor substrate 12 over word lines 14 and bit lines 26. An example preferred material includes doped silicon dioxide, such as borophosphosilicate glass (BPSG) deposited to an exemplary thickness range of from about 10,000 Angstroms to about 30,000 Angstroms, and is preferably composed to consist essentially of a doped silicon dioxide. Preferably, as shown, such comprises an outer planar surface 32.

Referring to Figs. 3 and 4, a portion of dielectric/insulative well forming layer 30 is removed to form at least one well 34 within well forming layer 30. Such patterning and removal most preferably occurs by photolithography whereby the area outside of well portion 34 is masked with photoresist, and a timed etched is preferably then conducted of layer 30 using a chemistry substantially selective to not remove the photoresist to form the illustrated well 34. Well 34 includes a periphery 35, which peripherally defines an outline of a memory array area and an area 36 peripheral and laterally outward of well 34 which comprises memory peripheral circuitry area. Well 34 also includes a base 38 which, in the preferred illustrated embodiment, is substantially planar. The etch to produce to the illustrated well 34 is preferably timed to provide a lowestmost portion 38 thereof which is received above word line caps 22 by at least 2000 Angstroms. Further, lowestmost portion 38 is preferably received above outermost tops of digit lines 26 by at least 1000 Angstroms and preferably less than 4000 Angstroms. A more preferred distance between base 38 and the outermost tops of the digit lines is from about 2500 Angstroms to about 3500 Angstroms, with 3000 Angstroms being a specific preferred distance.

Referring to Fig. 5, an etch stop layer 39 (preferably dielectric) is preferably deposited over well forming layer 30 outward of and to within well 34 to less than completely fill well 34. An exemplary and preferred material for layer 39 is silicon nitride, with an exemplary

preferred deposition thickness being from about 40 Angstroms to about 125 Angstroms, with from about 50 Angstroms to 70 Angstroms being more preferred. Such provides an insulative layer 39/30 outermost surface 40 which, in the illustrated and preferred embodiment, is substantially planar laterally outside of well 34.

Referring to Fig. 6, a storage node forming layer 42 is formed over etch stop layer 39 laterally outward of and to within well 34 to overfill well 34. Layer 42 preferably comprises a dielectric material, with BPSG being but one example. In the depicted embodiment, storage node forming layer 42 is initially formed to be substantially non-planar.

Referring to Fig. 7, storage node forming layer 42 is planarized. Preferably, the planarization is such to be effective to leave etch stop layer 39 covered by storage node forming layer 42 of a thickness of at least about 1,000 Angstroms outside of well 34. Planarization might occur by resist-etch back, chemical-mechanical polishing, or any other existing or yet-to-be-developed planarizing technique.

Referring to Fig. 8, an array of capacitor storage node openings 44 is formed through storage node forming layer 42, through etch stop layer 39, and into well forming layer 30 through well base 38 within well 34. Storage node openings 44 are formed over storage node contact locations/plugs 24.

Referring to Fig. 9, a capacitor storage node layer 46 (preferably hemispherical grain polysilicon, HSG) is formed preferably be chemical

vapor depositing over storage node forming layer 42 to within capacitor storage node openings 44 to less than completely fill such openings.

Referring to Fig. 10, capacitor storage node layer material 46 has been removed outwardly of storage node forming layer 42 effective to form an array of storage node capacitor electrodes 47 in electrical connection with storage node contact locations/plugs 24. In the illustrated and preferred embodiment, storage node capacitor electrodes 47 comprise a portion which has a container shape, with the portion being formed to be partially received within well forming layer 30 through the base openings within well 34. Non-container capacitor electrode constructions are also of course contemplated. Removal can occur by any of a number of techniques, with chemical-mechanical polishing being preferred. Capacitor storage node containers 47 have topmost surfaces 48 which, in the preferred embodiment, are received elevationally proximate outermost surface 40 of insulative layer 39/30. In the context of this document, "elevationally proximate" means elevationally within 50 Angstroms. In the illustrated and preferred embodiment, topmost surfaces 48 are received elevationally above substantially planar outermost surface 40 by less than 50 Angstroms. In preferred embodiments, exactly elevationally coincident or elevationally below are also contemplated, although not as preferred as that depicted in the drawings.

Referring to Fig. 11, at least some of capacitor storage node forming layer 42 is removed from within well 34. Preferably, such

removal occurs by chemical etching using a chemistry which is substantially selective to remove capacitor storage node forming layer 42 relative to etch stop layer 39, and as well exposes lateral outer container surface area 49 of capacitor containers 47. As illustrated and preferred, substantially all of capacitor storage node forming layer 42 is shown as having been etched from the substrate using dielectric etch stop layer 39 as an etch stop. Where layer 42 comprises BPSG and layer 39 comprises silicon nitride, an exemplary chemistry is dilute HF at a 10:1 volume ratio.

Referring to Fig. 12, a capacitor dielectric layer 50 and a capacitor cell electrode layer 52 are formed over capacitor storage node containers 47, including outer surface area 49.

Such provides but one example of forming an array of memory cell capacitors within well 34 over word lines 14 and digit lines 26. Peripheral circuitry 55 is formed within peripheral circuit area 36 and is operatively designed and configured to write to and read from the memory array, as is conventional or as yet-to-be-developed. Exemplary existing peripheral dynamic random access memory circuitry includes sense amplifier elements, equilibration and bias circuits, isolation devices, input/output transistors, etc. Exemplary devices 55 are shown only diagrammatically, as the peripheral circuitry placement, not the actual circuitry itself, is only what is germane to aspects of this invention.

Referring to Fig. 13, a planarized dielectric layer 56 and exemplary metal line/wiring components 58 are shown as being fabricated.

The illustrated exemplary embodiment, by way of example only and in no way by way of limitation, effectively elevationally recesses the memory array and thereby the vertically elongated memory array capacitors compared to the memory peripheral circuitry area. The outer surface of insulative layer 39/30 thereby provides a base which is preferably elevationally proximate or coincident with the tops of the storage nodes of the memory cell capacitors upon or through which the peripheral circuitry can be fabricated.

Further, the illustrated exemplary embodiment, by way of example only and not by way of limitation, also facilitates prevention of an existing processing problem known as oxidation punch-through. Punch-through results from oxygen penetration into lower substrate areas during wafer fabrication and undesired oxidation of underlying conductive components. Prior art capacitor fabrication methods have typically contended with punch-through by the silicon nitride barrier function of the capacitor dielectric material which typically comprises at least part of the capacitor dielectric layer. The nitride serves as a barrier to oxygen diffusion in subsequent steps which can undesirably form insulative oxides on circuitry material. Yet existing designs continue to push the effective thickness of the capacitor dielectric silicon nitride layer ever thinner such that suitable nucleation all over the wafer and

barrier properties typically will not occur. In the illustrated preferred embodiment, etch stop layer 39 is ideally fabricated of a diffusion barrier material, such as silicon nitride, and can be deposited to a suitable thickness (i.e., at least 50 Angstroms) to desirably form both an etch stop barrier layer function and an oxygen diffusion barrier layer during circuitry fabrication.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.